Public Products List

PCN Title : New material set in ST Boukoura on SO8 package (Voltage Reference) - General Purpose Analog products

PCN Reference : AMG/16/9849

PCN Created on : 16-Jun-2016

Subject : Public Products List

Dear Customer,

Please find below the Standard Public Products List impacted by the change.

TL431IDT	TL431CDT	TL431ACDT
TL1431IDT	TL431AIDT	TL1431CDT
TL1431ACDT		

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PRODUCT/PROCESS
CHANGE NOTIFICATION

PCN AMG/16/9849

Analog & MEMS Group

New material set in ST Bouskoura for SO8 package
Voltage reference – General Purpose Analog Division

WHAT:

Progressing on the activities related to quality continuous improvement, ST is glad to announce a new material set for SO8 packages produced in ST Bouskoura.
Please find more information related to material change in the table here below

Material	Current process	Modified process	Comment
Diffusion location	ST Ang Mo Kio (Singapore)	ST Ang Mo Kio (Singapore)	No change
Assembly location	ST Bouskoura	ST Bouskoura	No change
Molding compound	Sumitomo G700K	Sumitomo G700KC	Similar grade version more adapted to high density frame
Die attach	Ablestick 8601-S25	Ablestick 8601-S25	No change
Leadframe	Copper preplated NiPdAgAu standard density	Copper preplated ag spot High density	Move to Sn plating to solve some sporadic discoloration issues
Wire	Copper 1 mil	Copper 1 mil	No change
Plating	NiPdAgAu	Sn	Sn plating already running for standard product for more than 3 year on SO package and will allow to solve sporadic discoloration issues sawn on NiPdAgAu plating

Samples of vehicle test are available now and other samples will be launched upon customer's request. Please submit requests for samples within 30 days of this notification.

WHY:

This material change will contribute to ST's continuous quality product improvement and ensure a consistent assembly process through all the SO production lines.

HOW:

The qualification program consists mainly of comparative electrical characterization and reliability tests.

You will find here after the qualification test plan which summarizes the various test methods and conditions that ST uses for this qualification program.

WHEN:

The new material set will be implemented in Q3/2016 in Bouskoura.

Marking and traceability:

Unless otherwise stated by customer's specific requirement, the traceability of the parts assembled with the new material set will be ensured by new internal sales type, date code and lot number.

The second level interconnect, printed on label will move from e4 to e3.

The changes here reported will not affect the electrical, dimensional and thermal parameters keeping unchanged all the information reported on the relevant datasheets.
There is -as well- no change in the packing process or in the standard delivery quantities.

Lack of acknowledgement of the PCN within 30 days will constitute acceptance of the change. After acknowledgement, lack of additional response within the 90 day period will constitute acceptance of the change (Jedec Standard No. 46-C).
Shipments may start earlier with the customer's written agreement.

Reliability Report

New Halogen free material set for SO8 in ST Bouskoura for standard products

General Information	
Product Line	*0393, 0339, 0431*
Product Description	Dual comparator, bipolar, Quad comparator bipolar, Voltage Reference
P/N	*LM2903YDT, LM2901YDT, TL431CDT*
Product Group	*AMG*
Product division	*General Purpose Analog &RF*
Package	*SO8/14*
Silicon Process technology	*Bipolar*

Locations	
Wafer fab	*ST Singapore*
Assembly plant	*ST Bouskoura (Morocco)*
Reliability Lab	*ST Grenoble, ST Bouskoura*

TABLE OF CONTENTS

1 APPLICABLE AND REFERENCE DOCUMENTS

Document reference	Short description
AEC-Q100	Stress test qualification for automotive grade integrated circuits
AEC-Q101	Stress test qualification for automotive grade discrete semiconductors
JESD47	Stress-Test-Driven Qualification of Integrated Circuits

2 GLOSSARY

DUT	Device Under Test
PCB	Printed Circuit Board
SS	Sample Size

3 RELIABILITY EVALUATION OVERVIEW

3.1 Objectives

To qualify a new material set for SO8 package in ST Bouskoura (Sumitomo G700KC which is an evolution of Sumitomo G700K already in use in Bouskoura and move from NiPdAgAu preplating to Sn postplating) for AMG (Analog & Mems group).

3.2 Conclusion

Qualification Plan requirements have been fulfilled without issue. It is stressed that reliability tests have to show that the devices behave correctly against environmental tests (no failure). Moreover, the stability of electrical parameters during the accelerated tests have to demonstrate the ruggedness of the products and safe operation, which is consequently expected during their lifetime.

4 DEVICE CHARACTERISTICS

4.1 Device description

LM2903YDT

life.augmented

LM2903

Low-power dual voltage comparator

Datasheet - production data

N
DIP8
(plastic package)

D
SO8
(plastic micropackage)

P
TSSOP8
(thin shrink small outline package)

S
MiniSO8
(plastic micropackage)

DFN8 2x2 mm
(plastic micropackage)

Features

- Wide single supply voltage range or dual supplies +2 V to +36 V or ±1 V to ±18 V
- Very low supply current (0.4 mA) independent of supply voltage (1 mW/comparator at +5 V)
- Low input bias current: 25 nA typ.
- Low input offset current: ±5 nA typ.
- Input common-mode voltage range includes negative rail
- Low output saturation voltage: 250 mV typ. (I_O = 4 mA)
- Differential input voltage range equal to the supply voltage
- TTL, DTL, ECL, MOS, CMOS compatible outputs
- Automotive qualification

Related products

- See LM2903W for similar device with higher ESD performances
- See LM2903H for similar device with operating temperature up to 150 °C

Description

This device consists of two independent low-power voltage comparators designed specifically to operate from a single supply over a wide range of voltages. Operation from split power supplies is also possible.

In addition, the device has a unique characteristic in that the input common-mode voltage range includes the negative rail even though operated from a single power supply voltage.

LM2901YDT,

LM2901

Low-power quad voltage comparator

Features

- Wide single supply voltage range or dual supplies for all devices: +2 V to +36 V or ±1 V to ±18 V
- Very low supply current (1.1 mA) independent of supply voltage (1.4 mW/comparator at +5 V)
- Low input bias current: 25 nA typ.
- Low input offset current: ±5 nA typ.
- Input common-mode voltage range includes negative rail
- Low output saturation voltage: 250 mV typ. (I_O = 4 mA)
- Differential input voltage range equal to the supply voltage
- TTL, DTL, ECL, MOS, CMOS compatible outputs

N
DIP14
(Plastic package)

D
SO-14
(Plastic micropackage)

P
TSSOP14
(Thin shrink small outline package)

Q4
QFN16 3x3
(Plastic micropackage)

Description

This device consists of four independent precision voltage comparators, which are designed specifically to operate from a single supply over a wide range of voltages. Operation from split power supplies is also possible.

These comparators also have a unique characteristic in that the input common-mode voltage range includes the negative rail even though operated from a single power supply voltage.

TL431
TL432

Programmable voltage reference

Datasheet – production data

Features

- Adjustable output voltage: 2.5 to 36 V
- Sink current capability: 1 to 100 mA
- Typical output impedance: 0.22 Ω
- 1% and 2% voltage precision
- Automotive temp. range - 40 °C to +125 °C

Applications

- Power supply
- Industrial
- Automotive

Description

The TL431 and TL432 are programmable shunt voltage references with guaranteed temperature stability over the entire operating temperature range. The device temperature range is extended for the automotive version from -40 °C up to +125 °C. The output voltage can be set to any value between 2.5 and 36 V with two external resistors. The TL431 and TL432 operate with a wide current range from 1 to 100 mA with a typical dynamic impedance of 0.22 Ω.

Z
TO-92
(Plastic package)

L
SOT23-3

L
SOT23-5

C
SOT323-6

D
SO-8
(Batwing plastic micropackage)

4.2 Construction note

	P/N *LM2903YDT*	**P/N *LM2901YDT***	**P/N TL431CDT**
Wafer/Die fab. information			
Wafer fab manufacturing location	ST Singapore	ST Singapore	ST Singapore
Technology	Bipolar	Bipolar	HBIP40V
Die finishing back side	RAW SILICON	RAW SILICON	HBIP40V
Die size (microns)	950 x 870 µm	1370x1270	900x620µm
Bond pad metallization layers	AlSiCu	AlSiCu	AlSiCu
Passivation type	Nitride	Nitride	PVAPOX/NITRIDE
Wafer Testing (EWS) information			
Electrical testing manufacturing location	ST Singapore	ST Singapore	ST Singapore
Tester	ASL1K	ASL1K	ASL1K
Assembly information			
Assembly site	ST Bouskoura	ST Bouskoura	ST Bouskoura
Package description	SO8	SO14	SO8
Molding compound	EME G700KC	EME G700KC	EME G700KC
Frame material	Cu	Cu	Cu
Die attach process	Epoxy Glue	Epoxy Glue	Epoxy Glue
Die attach material	8601S-25	8601S-25	8601S-25
Wire bonding process	Thermosonic ball bonding	Thermosonic ball bonding	Thermosonic ball bonding
Wires bonding materials/diameters	Cu 1 mil	Cu 1 mil	Cu 1 mil
Lead finishing process	electroplating	electroplating	electroplating
Lead finishing/bump solder material	Matte tin	Matte tin	Matte tin
Final testing information			
Testing location	ST Bouskoura	ST Bouskoura	ST Bouskoura
Tester	ASL1K	ASL1K	ASL1K

5 TESTS RESULTS SUMMARY

5.1 Test vehicle

Lot #	Process/ Package	Product Line	Comments
1	Bipolar/SO8	0393	CZ53005LRP CZ53005LRN CZ53005LRQ CZ53005LRR CZ53005LRM CZ53005LRL
2	Bipolar/SO14	0339	CZ52405FR6 CZ52405FR7 CZ52405FR8
12	HBIP40V	0431	CZ54406NRQ

5.2 Test plan and results summary

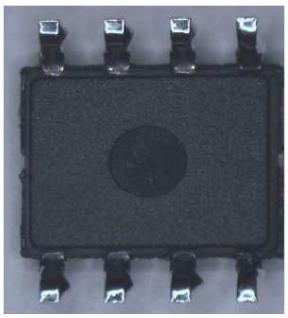
Test	PC	Std ref.	Conditions	SS	Steps	Failure/SS			Note
						Lot 1 0393	Lot 2 0339	Lot12 0431	
HTB/ HTOL	N	JESD22 A-108	Ta = 150°C, BIAS		168 H	0/78	0/78	0/77	* Tj=125°C
					500 H	0/78	0/78	0/77	
					1000 H	0/78	0/78	0/77	
ELFR	N	JESD22 A-008	Ta = 125°C, BIAS			0/450	0/450		
HTSL	N	JESD22 A-103	Ta = 150°C		168 H	6X0/77	3x0/77	0/45	(1)
					500 H	6X0/77	3x0/77	0/45	
					1000 H	6X0/77	3x0/77	0/45	
					2000H		3x0/77		
PC		JESD22 A-113	Drying 24 H @ 125°C Store 168 H @ Ta=85°C Rh=85% Over Reflow @ Tpeak=260°C 3 times		Final	PASS	PASS	PASS	
AC	Y	JESD22 A-102	Pa=2Atm / Ta=121°C		96 H 168H	6x0/77	3x0/77	0/77 0/77	(1)
TC	Y	JESD22 A-104	Ta = -65°C to 150°C		100 cy	6x0/77	3x0/77	0/77	(1)
					200 cy	6x0/77	3x0/77	0/77	
					500 cy	6x0/77	3x0/77	0/77	
					1000cy	6x0/77	3x0/77		
THB	Y	JESD22 A-101	Ta = 85°C, RH = 85%, BIAS		168 H		0/78	0/77	
					500 H		0/78	0/77	
					1000 H		0/78	0/77	
ESD	N	AEC Q101-001, 002 and 005	CDM						
						0/3	0/3	0/3	
SD	N		After ageing 8h and 16h			Pass	Pass		

(1) Additional split lot to cover the whole assembly variability

Solderability:
Lot reference: CZ53005LRN,CZ53005LRQ, CZ53005LRR, CZ53005LRL

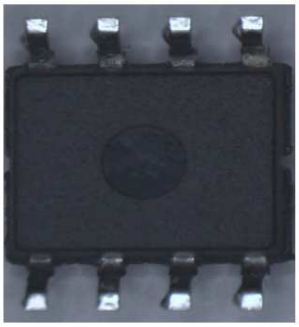
T0 solderability with SnPb bath and SnagCu bath 0 reject on 15 units:

After SnPb



No solderability issue on all units after

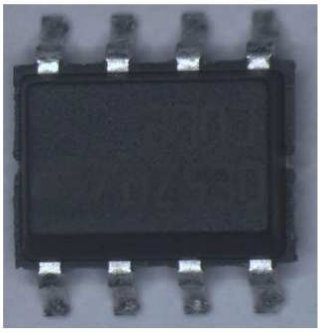
After SnAg

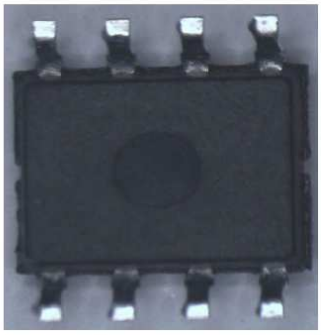


No solderability issue on all units after

After 8h 85°C/85%RH solderability with SnPb bath and SnAgCu bath 0 reject on 15 units:

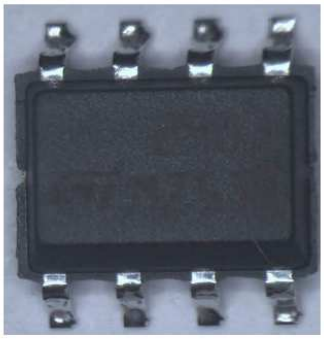
After SnAg

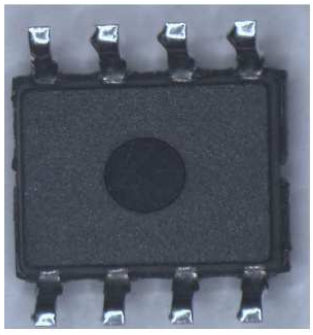




No solderability issue on all units after

After SnPb

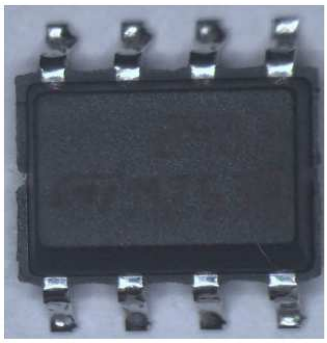


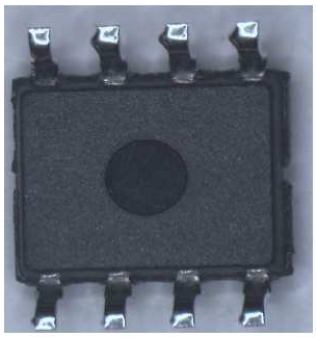


No solderability issue on all units after

After 16h 150°C, solderability with SnPb bath and SnAgCu bath 0 reject on 15 units:

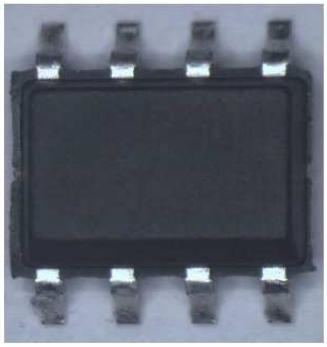
After SnPb

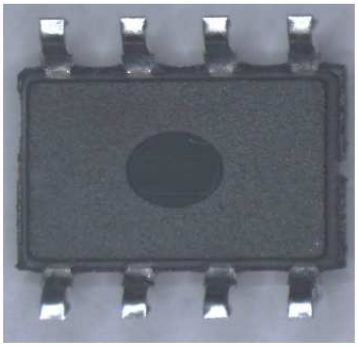




No solderability issue on all units after

After SnAg





No solderability issue on all units after

Tin Surface Finish Acceptance Testing per JESD201 & JESD 22A121

P.Crema

Assembled :
STM Marocco Bouskoura

SO8L PMOS

DISCLAIMER

The whisker test procedures identified in this report are used for determining the presence of tin whiskers and are performed by STMicroelectronics Inc., pursuant to current industry accepted JEDEC standards. The whisker test procedures used herein are unproven and may produce inconclusive results. STMicroelectronics Inc. makes no representation, warranty or guarantee of any kind with respect to the field performance, quality or freedom from whisker-related failures, of any package tested by STMicroelectronics using these procedures.

General Information

Package		**SO8L** PMOS
Factory		STMicroelectronics Morocco
Factory Location		Bouskoura
Lead Frame Alloy		Copper : O194
Lead Finish		Matte Tin
Tin Thickness		7 – 20 um on leads
Plating Vendor		Atotech GmbH
Plating Machine		MECO
Plating Chemistry		Stannopure HSM
Mitigation		Post Plating Bake within 24hrs @150 for 1 hr.

Chemical Plating process information

September 11 , 2008					
Description	**Process**	**Volume tank (liter)**	**Make up Concentration (g/l or ml/l)**	**Density**	**Quantity used for the bath**
Electro cleaner	Puronon RTR	80	100g/l		8kg
Activation Ni/Fe					
Activation Cu	Descabase Cu	80	50g/l		4kg
	H2SO4		30ml/l	1.61	3.36litre
Predip	MSA Special Acid HS	80	100ml/l	1.34	8litres
Tin plate	MSA Tin Solution HS 20	320	70g/l	1.53	81 litres
	MSA Special Acid HS		190 g/l	1.34	71 litres
	Stannopure HSM Additive HT		50ml/l	1	16litres
	Stannopure HSM Grain Refiner GF		15ml/l	1	4.8litres
	Antioxydant SN		5ml/l	1	1.6 litres
Neutral	Protectostan LF	80	100ml/l	1	8 litres
Stripper	Becastrip EL Part A	240	550ml/l	1.24	132 litres
	Becastrip EL Part B		20ml/l	1.53	4.8 litres

Plating equipment & process parameters

Equipment identification	Supplier	Type	Model
MECO 1	MECO	Continuous automatic plating	EPL 1200S

	Electro cleaner	Activation	Plating	Neutraliser
Temperature	50°C	RT	45°C	RT
Voltage /Ampérage	50A	30A	120A 120A 120A 120A	-
Belt speed	4.0 m/mn			

Pre Conditions

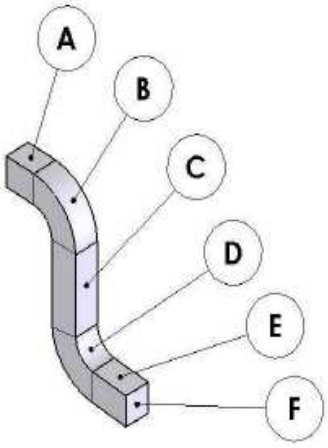
PreCondition	Conditions
No Pre condition	Ambient Only
Reflow (Single Pass)	215 deg C in air
Reflow (Single Pass)	245 – 260 deg C in air

Test plan

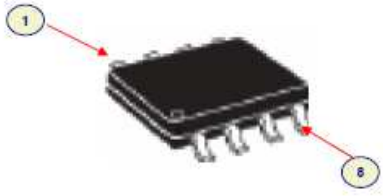
Test	Short description	Conditions
Thermal Cycling	TC	- 40℃ to + 85℃
High Humidity Storage	HT	55℃-85%RH
Controlled Ambient Storarge	RT	30℃-60%RH

Fig 1: Inspection Zones

Inspection: Top + 2 Sides



Lead identification



Temp. Cycles Whiskers inspection results

Optical inspection @ 50 X						
			n. of cycles			
Preconditioning	Device	Sample size	@ 0	@ 500	@1000	@1500
None	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers
215℃	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers
247℃	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers

Soak 30c/60%RH Whisker Inspection Results

Optical inspection @ 50 X							
			Time in hrs				
Preconditioning	Device	Sample size	@ 0	@ 1000	@2000	@3000	@4000
None	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
215℃	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
247℃	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers

Soak 55c/85%RH Whisker Inspection Results

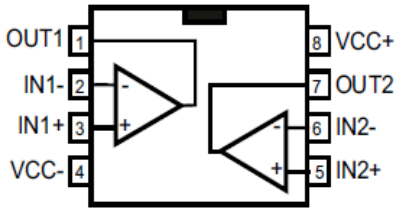
Optical inspection @ 50 X								
			Time in hrs					
Preconditioning	Device	Sample size	@ 0	@ 1000	@2000	@3000	@4000	Discounted lead
None	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
215℃	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
247℃	Lot 1	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
	Lot 2	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--
	Lot 3	4	No whiskers	No whiskers	No whiskers	No whiskers	No whiskers	--

6 ANNEXES

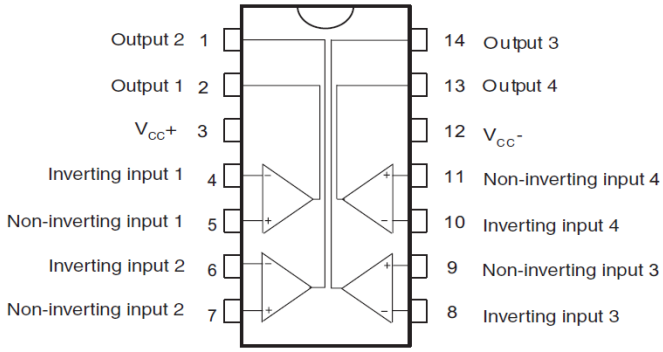
6.1 Device details

6.1.1 Pin connection

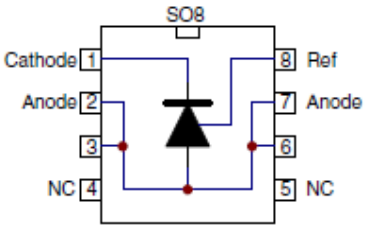
LM2903



LM2901

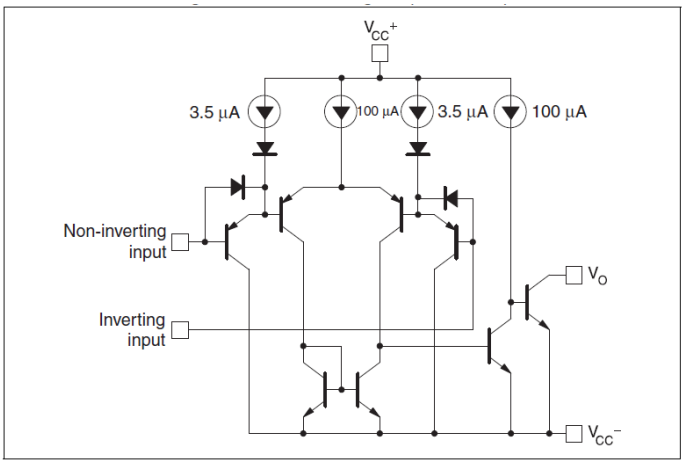


0431

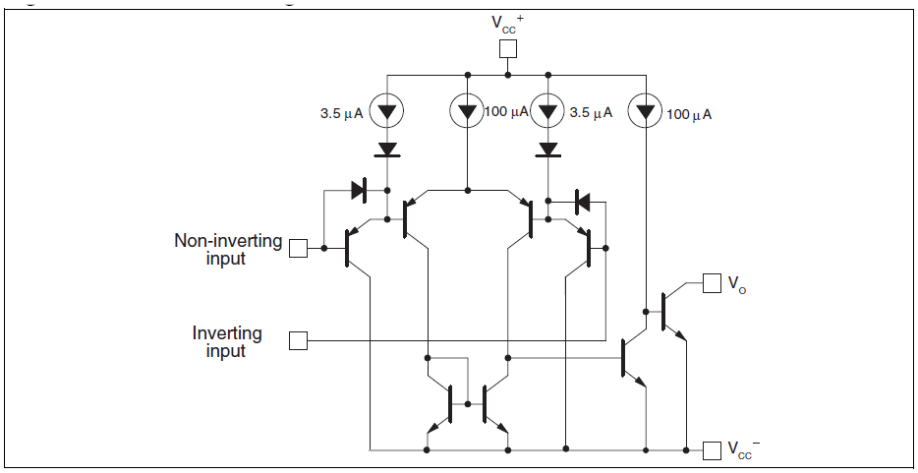


6.1.2 Block diagram

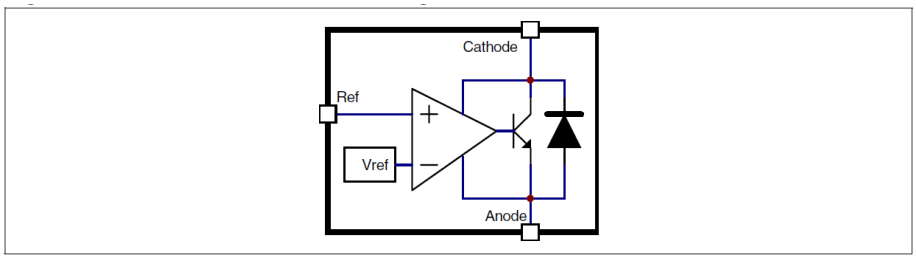
LM2903



LM2901



TL431



6.2 Tests Description

Test name	Description	Purpose
Die Oriented		
HTOL High Temperature Operating Life **HTB** High Temperature Bias	The device is stressed in static or dynamic configuration, approaching the operative max. absolute ratings in terms of junction temperature and bias condition.	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. The typical failure modes are related to, silicon degradation, wire-bonds degradation, oxide faults.
HTRB High Temperature Reverse Bias **HTFB / HTGB** High Temperature Forward (Gate) Bias	The device is stressed in static configuration, trying to satisfy as much as possible the following conditions: low power dissipation; max. supply voltage compatible with diffusion process and internal circuitry limitations;	To determine the effects of bias conditions and temperature on solid state devices over time. It simulates the devices' operating condition in an accelerated way. To maximize the electrical field across either reverse-biased junctions or dielectric layers, in order to investigate the failure modes linked to mobile contamination, oxide ageing, layout sensitivity to surface effects.
HTSL High Temperature Storage Life	The device is stored in unbiased condition at the max. temperature allowed by the package materials, sometimes higher than the max. operative temperature.	To investigate the failure mechanisms activated by high temperature, typically wire-bonds solder joint ageing, data retention faults, metal stress-voiding.
ELFR Early Life Failure Rate	The device is stressed in biased conditions at the max junction temperature.	To evaluate the defects inducing failure in early life.
Package Oriented		
PC Preconditioning	The device is submitted to a typical temperature profile used for surface mounting devices, after a controlled moisture absorption.	As stand-alone test: to investigate the moisture sensitivity level. As preconditioning before other reliability tests: to verify that the surface mounting stress does not impact on the subsequent reliability performance. The typical failure modes are "pop corn" effect and delamination.
AC Auto Clave (Pressure Pot)	The device is stored in saturated steam, at fixed and controlled conditions of pressure and temperature.	To investigate corrosion phenomena affecting die or package materials, related to chemical contamination and package hermeticity.
TC Temperature Cycling	The device is submitted to cycled temperature excursions, between a hot and a cold chamber in air atmosphere.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.

Test name	Description	Purpose
TF / IOL Thermal Fatigue / Intermittent Operating Life	The device is submitted to cycled temperature excursions generated by power cycles (ON/OFF) at T ambient.	To investigate failure modes related to the thermo-mechanical stress induced by the different thermal expansion of the materials interacting in the die-package system. Typical failure modes are linked to metal displacement, dielectric cracking, molding compound delamination, wire-bonds failure, die-attach layer degradation.
THB Temperature Humidity Bias	The device is biased in static configuration minimizing its internal power dissipation, and stored at controlled conditions of ambient temperature and relative humidity.	To evaluate the package moisture resistance with electrical field applied, both electrolytic and galvanic corrosion are put in evidence.
Other		
ESD Electro Static Discharge	The device is submitted to a high voltage peak on all his pins simulating ESD stress according to different simulation models. CBM: Charged Device Model HBM: Human Body Model MM: Machine Model	To classify the device according to his susceptibility to damage or degradation by exposure to electrostatic discharge.
LU Latch-Up	The device is submitted to a direct current forced/sunk into the input/output pins. Removing the direct current no change in the supply current must be observed.	To verify the presence of bulk parasitic effect inducing latch-up.